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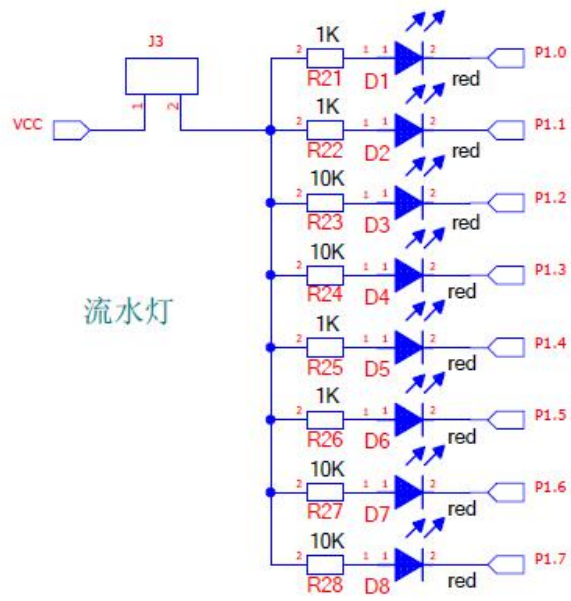
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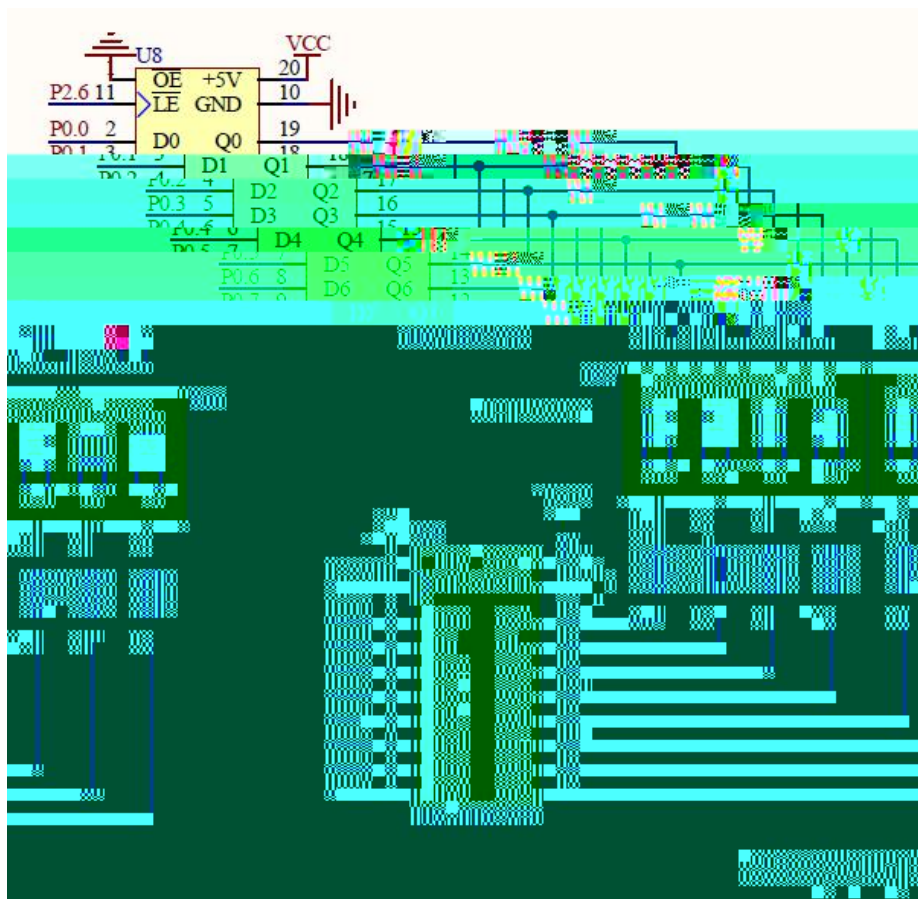








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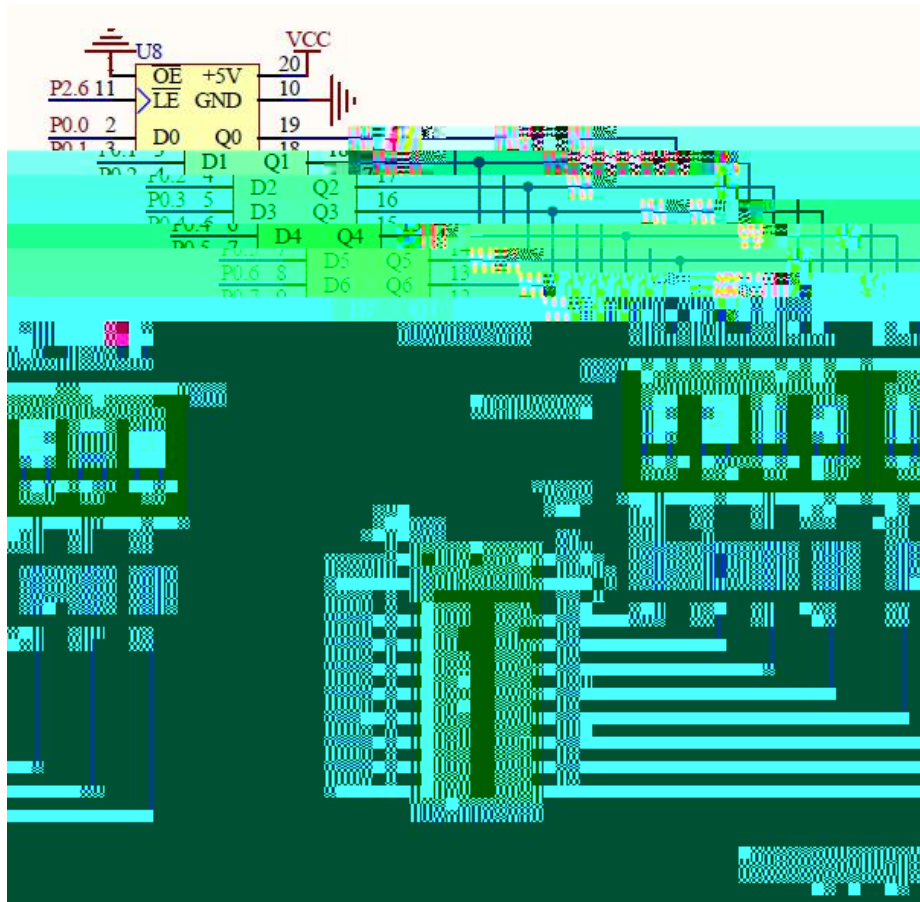
2

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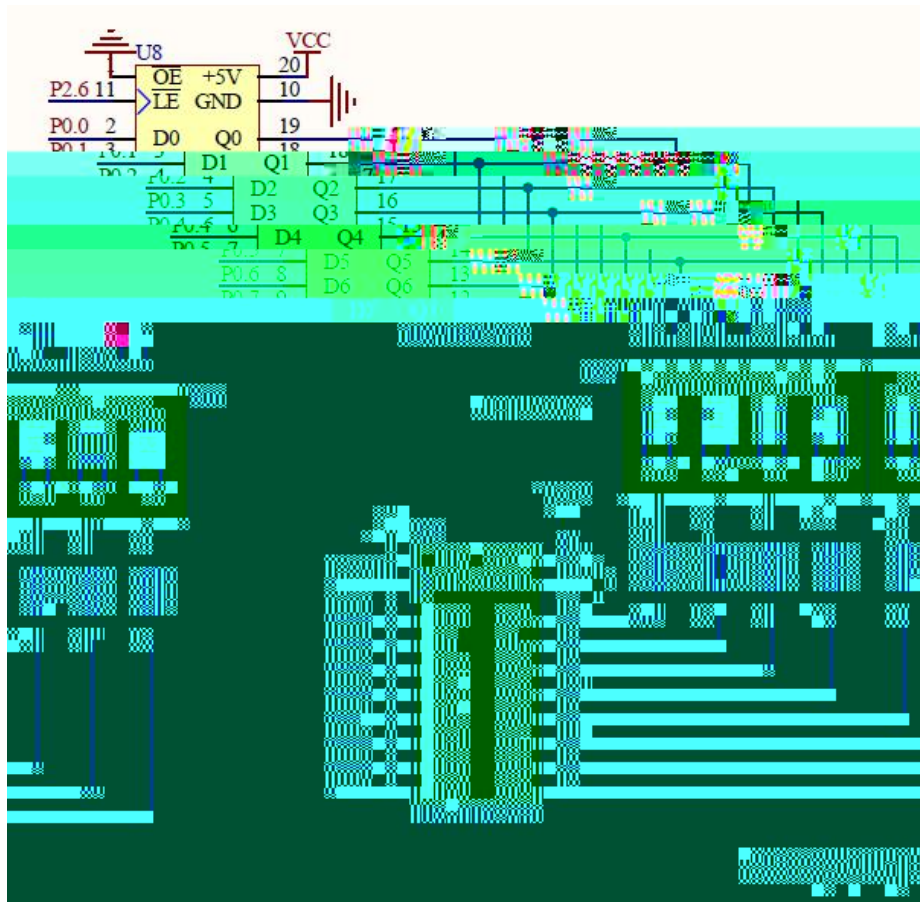
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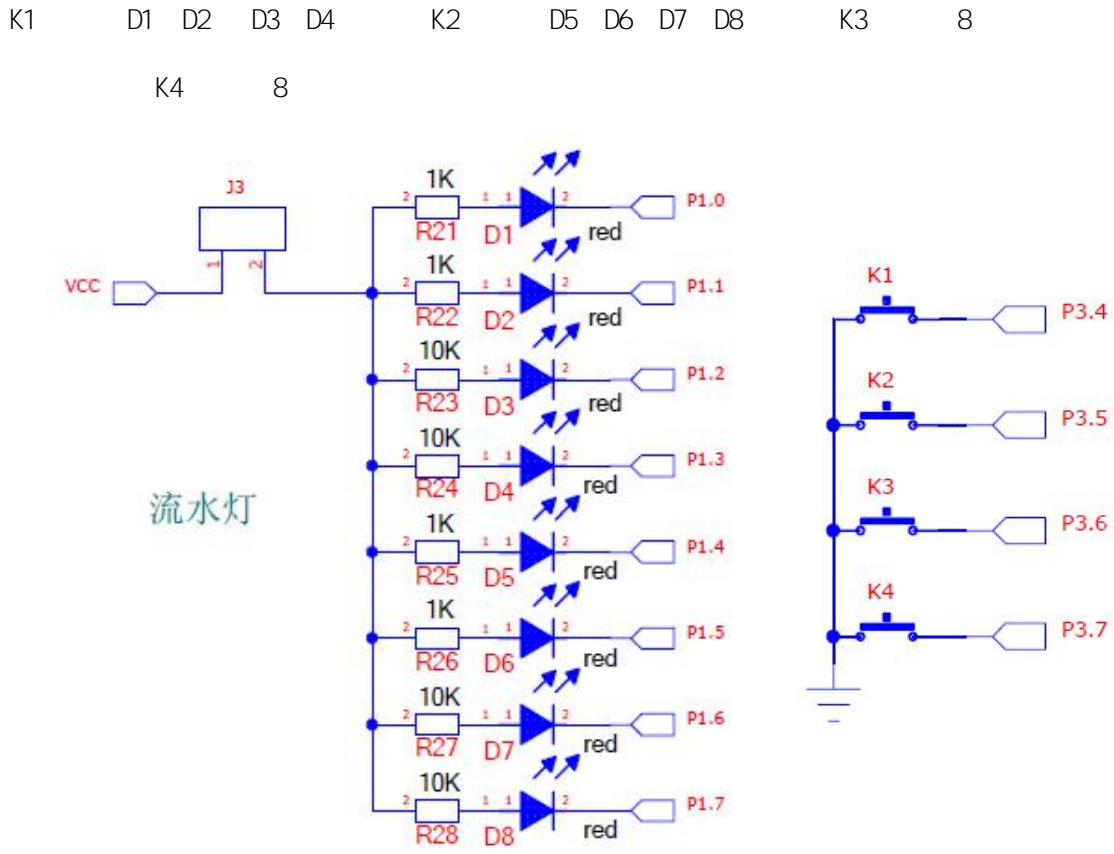
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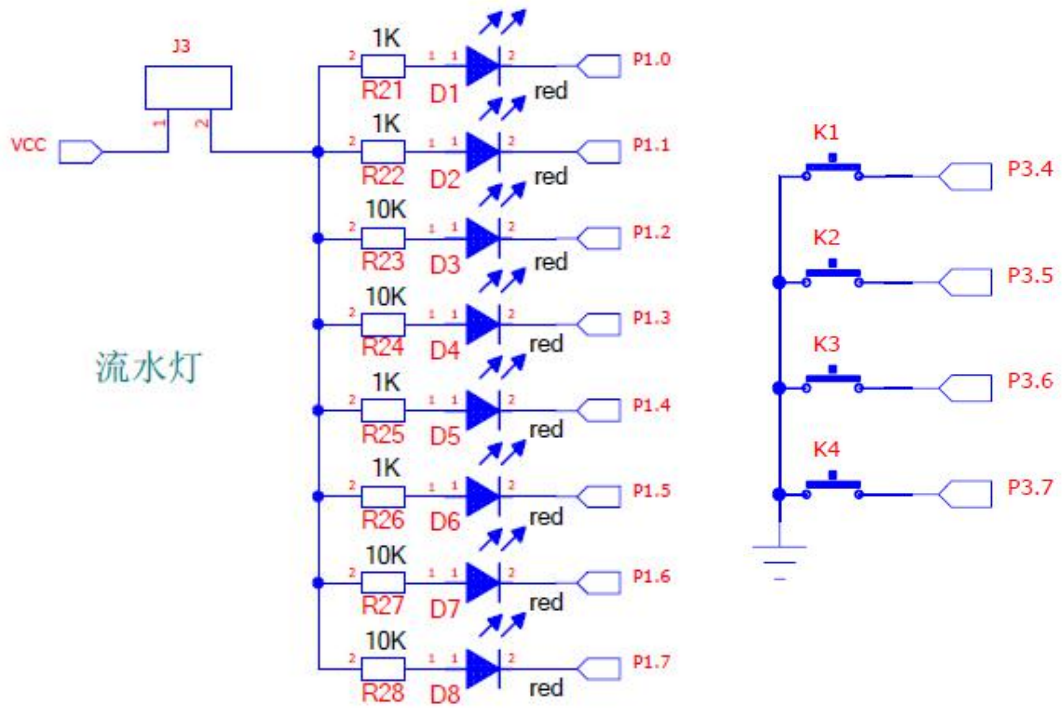
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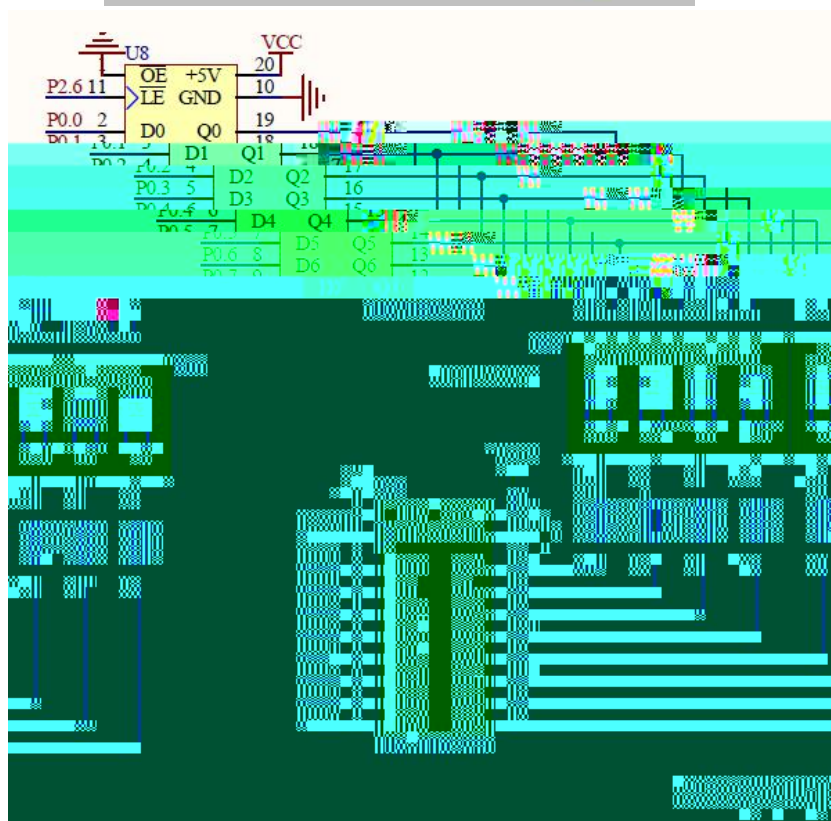
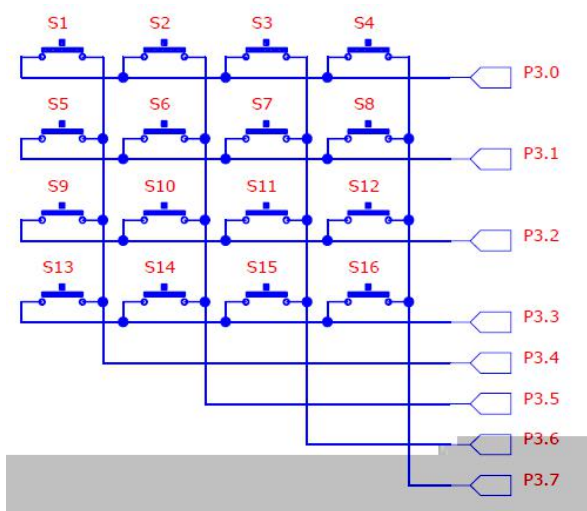
3



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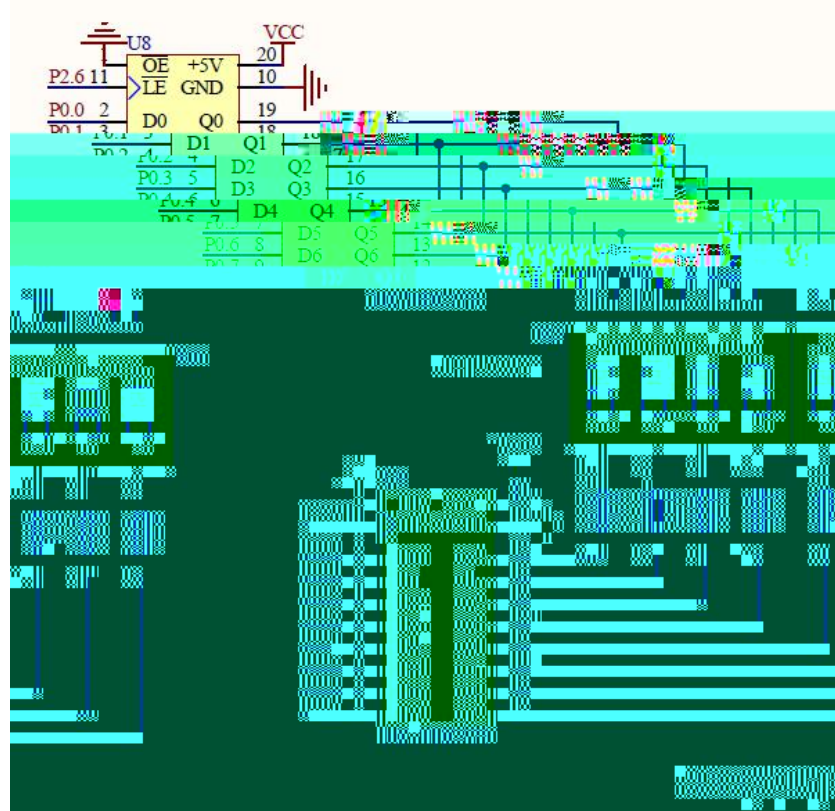
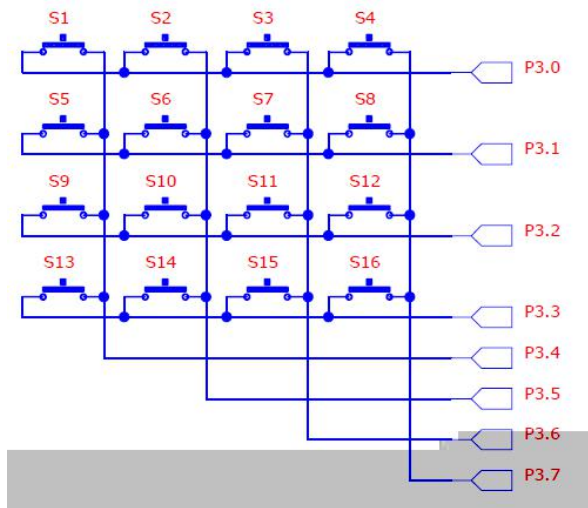
3

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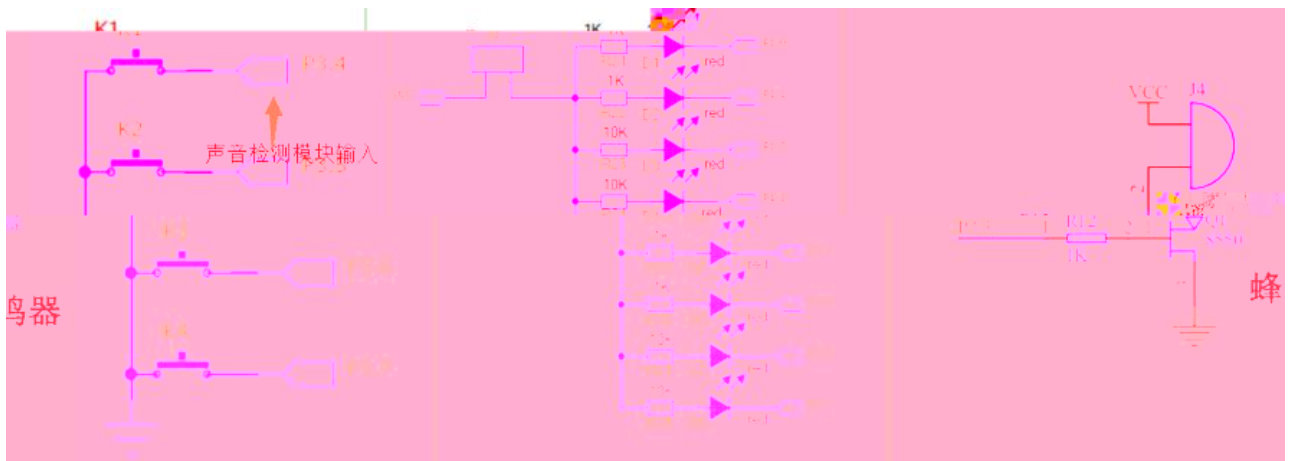
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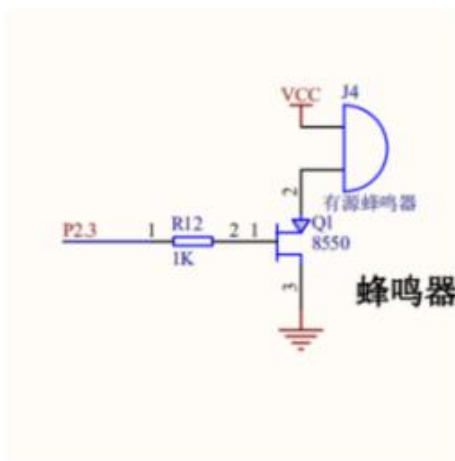
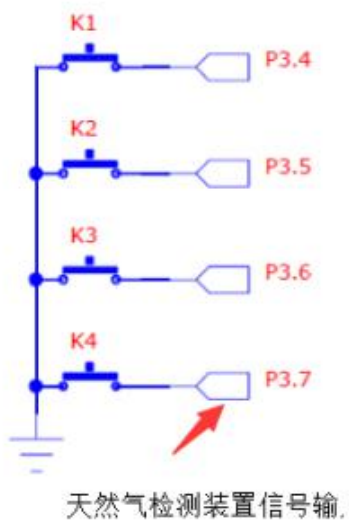
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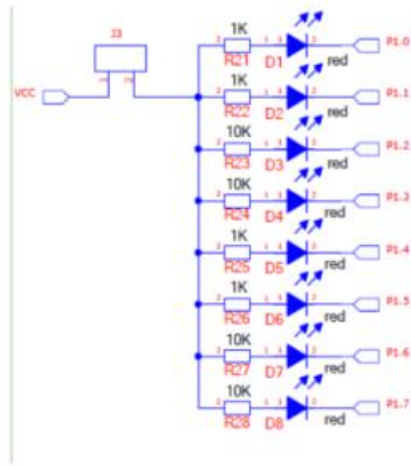
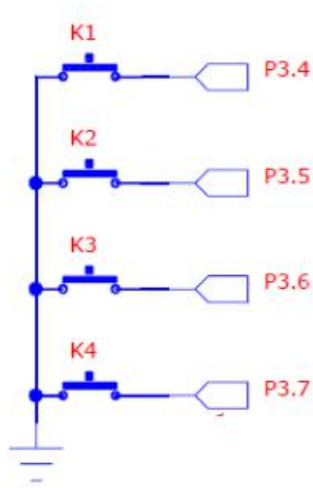
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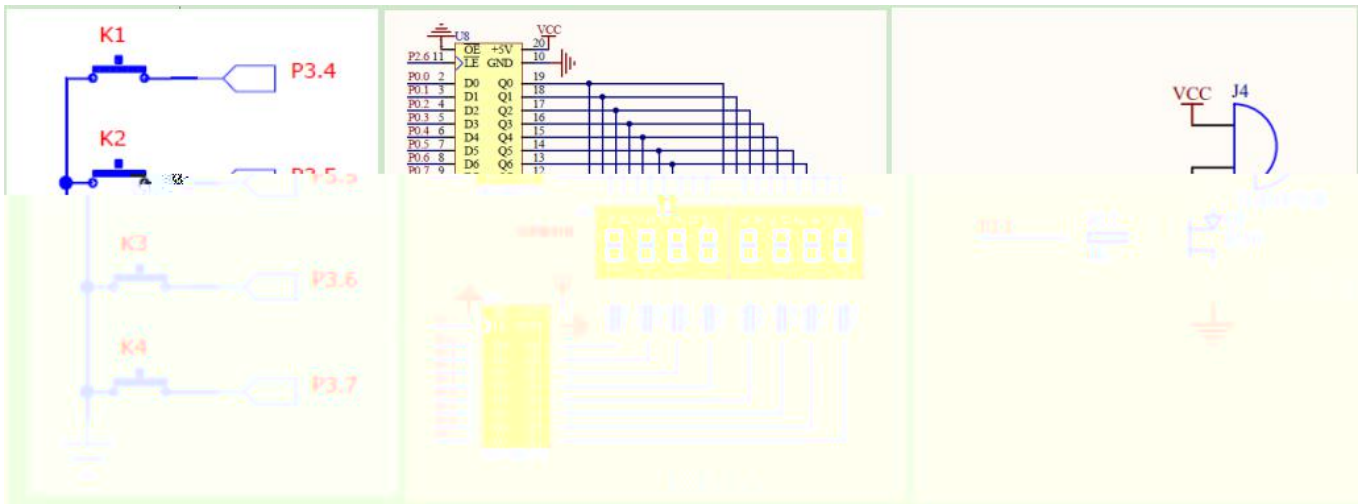
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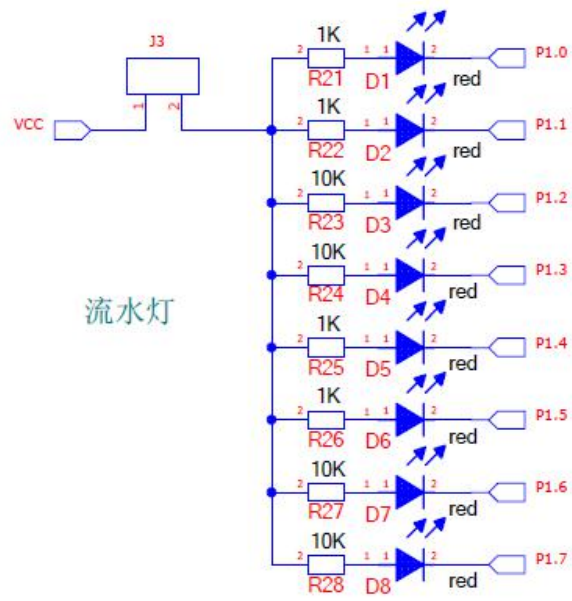
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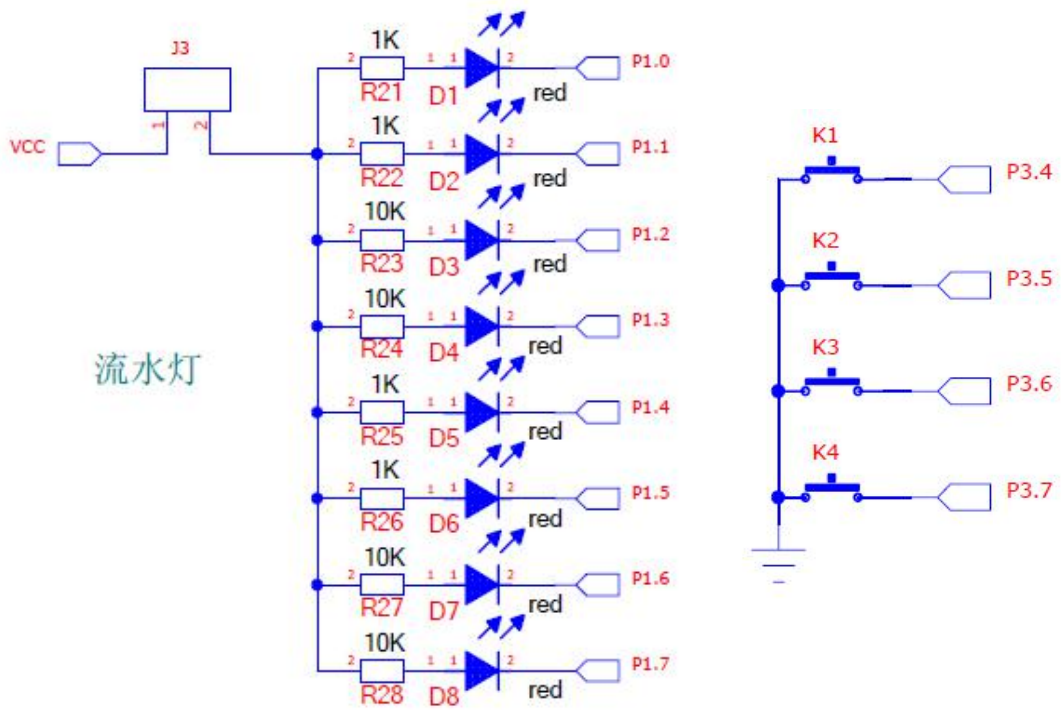
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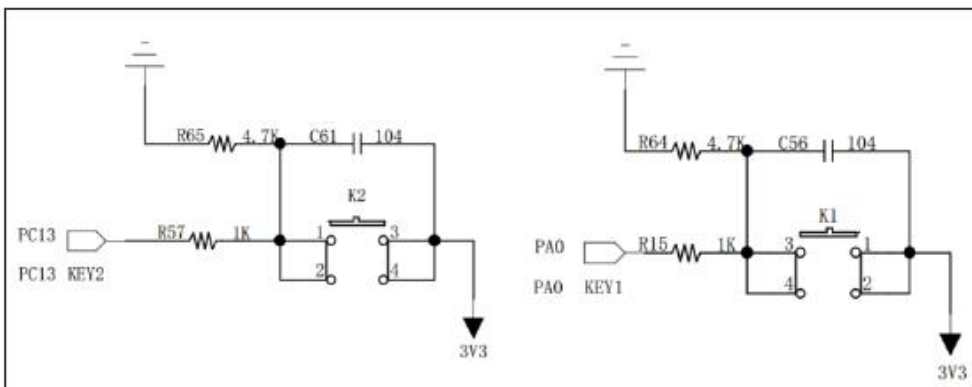
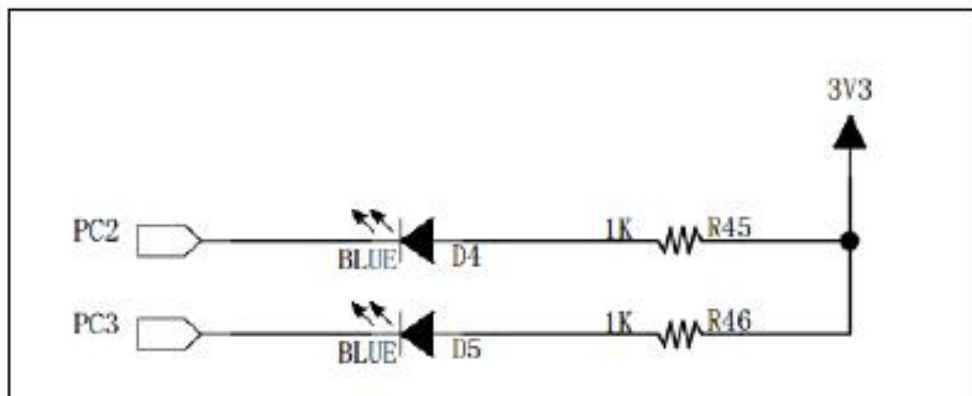
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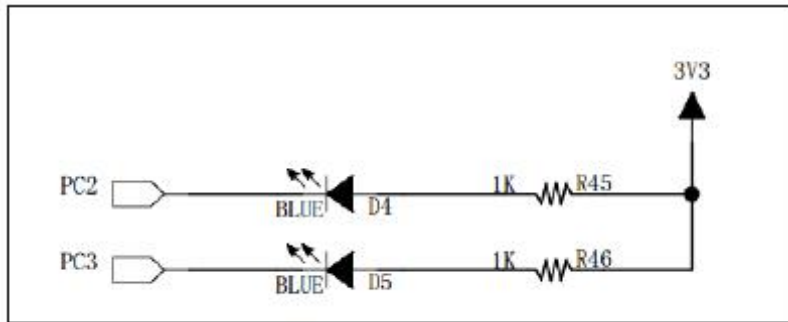
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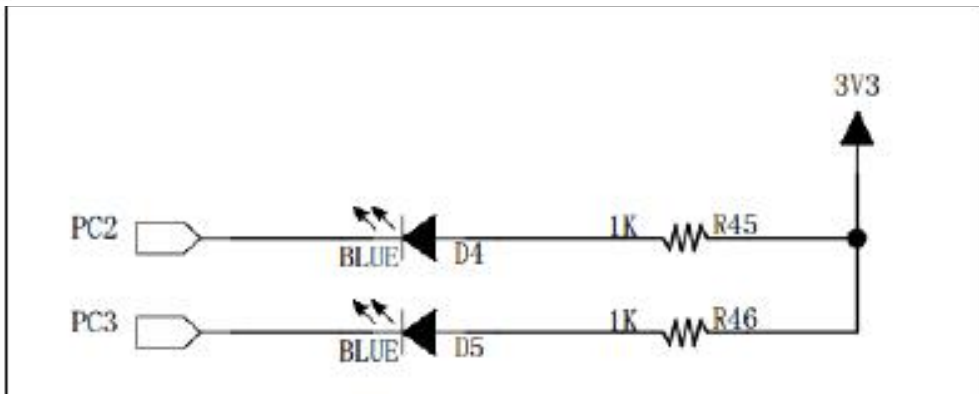
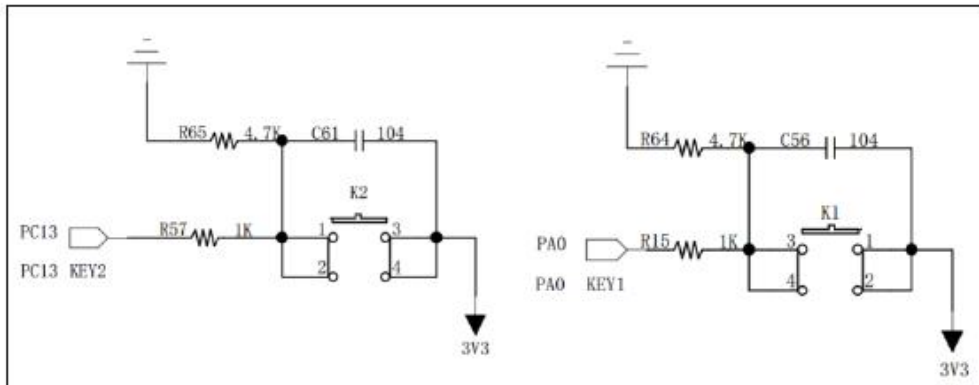
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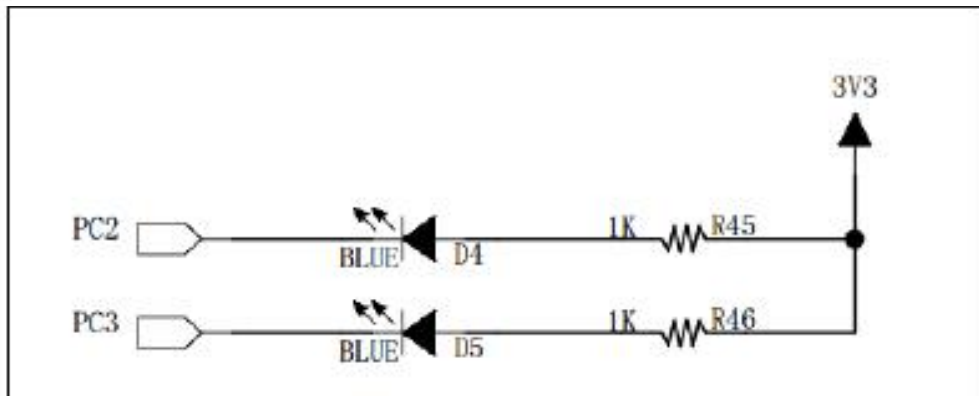
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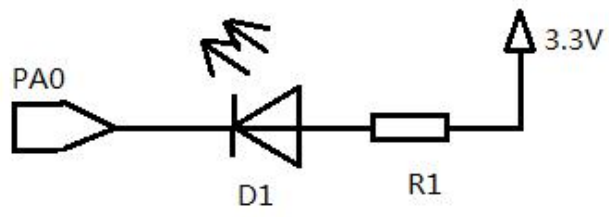
1	VBAT	VDD	64
2	PC13/ANT1	VSS	63
3	PC14/OSC32	PB9/TIM4_CH4/SDIO_D5	62
4	PC15/OSC32	PB8/TIM4_CH3/SDIO_D4	61
5	PD0/OSCIN	...	60
6	PD1/OSCOUT	...	59
7	NRST	PB7/I2C1_SDA/TIM4_CH2	58
8	PC0/ADC10	PB6/I2C1_SCL/TIM4_CH1	57
9	PC1/ADC11	PB5/I2C1_SMBA/SPI3_MOSI/I2S3_SD	56
10	PC2/ADC12	PB4/JNTRST/SPI3_MISO	55
11	PC3/ADC13	PB3/JTDO/SPI3_SCK/I2S3_CK	54
12	VSSA	PD2/U5_RX/TIM3_ETR/SDIO_CMD	53
13	VDDA	PC12/U5_TX/SDIO_CK	52
14	PA0/WKUP/ADC0/TIM2_CH1_ETR/TIM5_CH1/TIM8_ETR	PC11/U4_RX/SDIO_D3	51
15	PA1/ADC1/TIM2_CH2/TIM5_CH2	PC10/U4_TX/SDIO_D2	50
16	PA2/U2_TX/ADC2/TIM2_CH3/TIM5_CH3	PA15/JTDI/SPI3_NSS/I2S3_WS	49
17	PA3/U2_RX/ADC3/TIM2_CH4/TIM5_CH4	PA14/JTCK/SWCLK	48
18	VSS	vdd	47
19	VDD	VSS	46
20	PA4 SPI1 NSS/ADC4_DAC1	PA13 JTMS SWDIO	45
21	PA5 SPI1 SCK/ADC5_DAC2	PA12 CAN TX USBDF/TIM1_ETR	44
22	PA6 SPI1 MISO/ADC6/TIM3_CH1/TIM8_BRKIN	PA11 CAN RX USBDM/TIM1_CH4	43
23	PA7 SPI1 MOSI/ADC7/TIM3_CH2/TIM8_CH1N	PA10 U1 RX/TIM1_CH3	42
24	PC4 ADC14	PA9 U1 TX/TIM1_CH2	41
25	PC5 ADC15	PA8 TIM1_CH1/MCO	40
26	PB0 ADC8/TIM3_CH3/TIM8_CH2N	PC9 TIM8_CH4/SDIO_D1	39
27	PB1 ADC9/TIM3_CH4/TIM8_CH3N	PC8 TIM8_CH3/SDIO_D0	38
28	PB2 BOOT1	PC7 I2S3 MCK/TIM8_CH2/SDIO_D7	37
29	PB10 U3 TX/I2C2_SCL	PC6 I2S2 MCK/TIM8_CH1/SDIO_D8	36
30	PB11 U3 RX/I2C2_SDA	PB15 SPI2 MOSI/I2S2_SD/TIM1_CH3N	35
31	VSS	PB14 SPI2 MISO/TIM1_CH2N	34
32	VDD	PB13 SPI2 SCK/I2S2_CK/TIM1_CH1N	33
		PB12 SPI2 NSS/I2S2_WS/I2C2_SMBAL/TIM1_BRKIN	32

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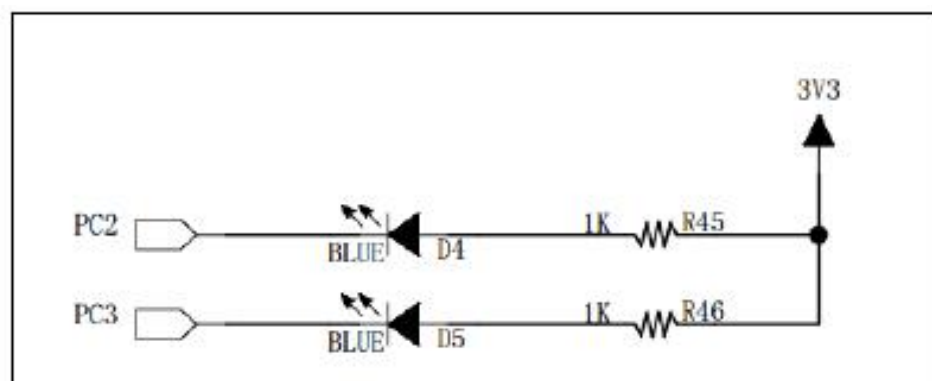
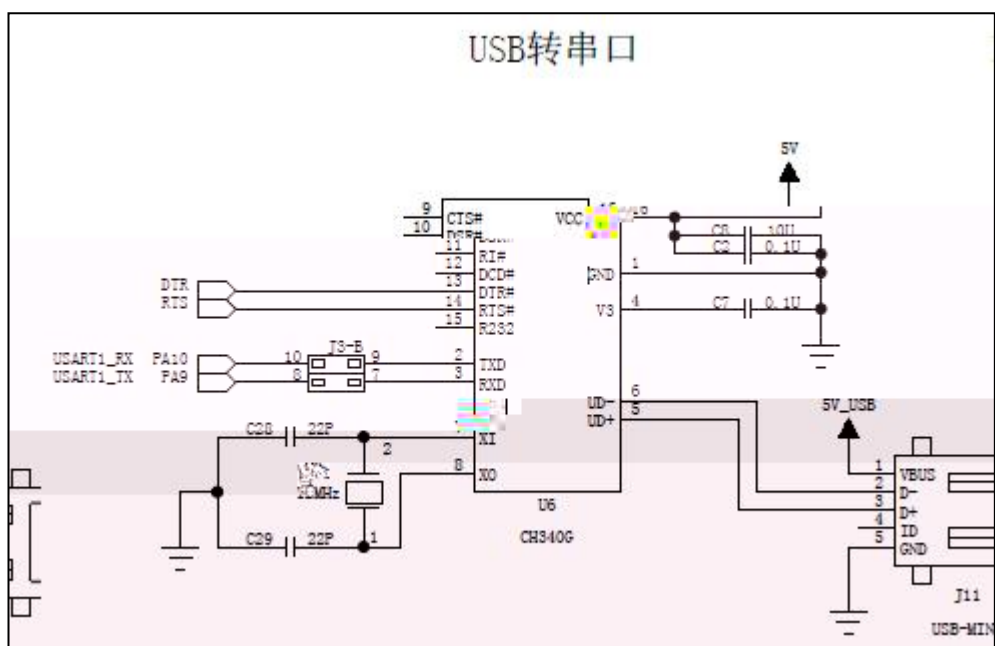
1	VBAT	VDD	64
2	PC13/ANT1	VSS	63
3	PC14/OSC32	PB9/TIM4_CH4/SDIO_D5	62
4	PC15/OSC32	PB8/TIM4_CH3/SDIO_D4	61
5	PD0/OSCIN	BOOT0	60
6	PD1/OSCOU	PB7/I2C1_SDA/TIM4_CH2	59
7	NRST	PB6/I2C1_SCL/TIM4_CH1	58
8	PC0/ADC10	PB5/I2C1_SMBA/SPI3_MOSI/I2S3_SD	57
9	PC1/ADC11	PB4/JNTRST/SPI3_MISO	56
10	PC2/ADC12	PB3/JTDO/SPI3_SCK/I2S3_CK	55
11	PC3/ADC13	PD2/U5_RX/TIM3_ETR/SDIO_CMD	54
12	VSSA	PC12/U5_TX/SDIO_CK	53
13	VDDA	PC11/U4_RX/SDIO_D3	52
14	PA0/WKUP/ADC0/TIM2_CH1_ETR/TIM5_CH1/TIM8_ETR	PC10/U4_TX/SDIO_D2	51
15	PA1/ADC1/TIM2_CH2/TIM5_CH2	PA15/JTDI/SPI3_NSS/I2S3_WS	50
16	PA2/U2_TX/ADC2/TIM2_CH3/TIM5_CH3	PA14/JTCK/SWCLK	49
17	PA3/U2_RX/ADC3/TIM2_CH4/TIM5_CH4	VDD	48
18	VSS	VSS	47
19	VDD	PA13/JTMS/SWDIO	46
20	PA4 SPI1_NSS/ADC4_DAC1	PA12/CAN_TX/USBCP/TIM1_ETR	45
21	PA5 SPI1_SCK/ADC5_DAC2	PA11/CAN_RX/USBCM/TIM1_CH4	44
22	PA6 SPI1_MISO/ADC6/TIM3_CH1/TIM8_BKIN	PA10/U1_RX/TIM1_CH3	43
23	PA7 SPI1_MOSI/ADC7/TIM3_CH2/TIM8_CH1N	PA9/U1_TX/TIM1_CH2	42
24	PC4/ADC14	PA8/TIM1_CH1/MCO	41
25	PC5/ADC15	PC9/TIM8_CH4/SDIO_D1	40
26	PB0/ADC8/TIM3_CH3/TIM8_CH2N	PC8/TIM8_CH3/SDIO_D0	39
27	PB1/ADC9/TIM3_CH4/TIM8_CH3N	PC7/I2S3_MCK/TIM8_CH2/SDIO_D7	38
28	PB2/BOOT1	PC6/I2S2_MCK/TIM8_CH1/SDIO_D6	37
29	PB10/U3_TX/I2C2_SCL	PB15/SPI2_MOSI/I2S2_SCK/TIM1_CH3N	36
30	PB11/U3_RX/I2C2_SDA	PB14/SPI2_MISO/TIM1_CH2N	35
31	VSS	PB13/SPI2_SCK/I2S2_CK/TIM1_CH1N	34
32	VDD	PB12/SPI2_NSS/I2S2_WS/I2C2_SMBAL/TIM1_BKIN	33

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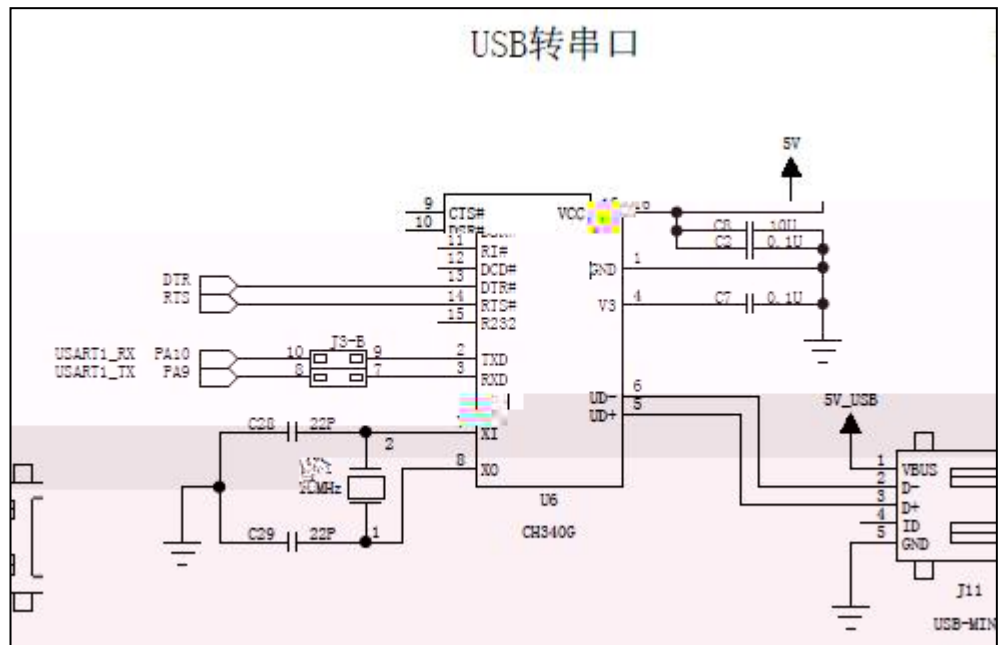


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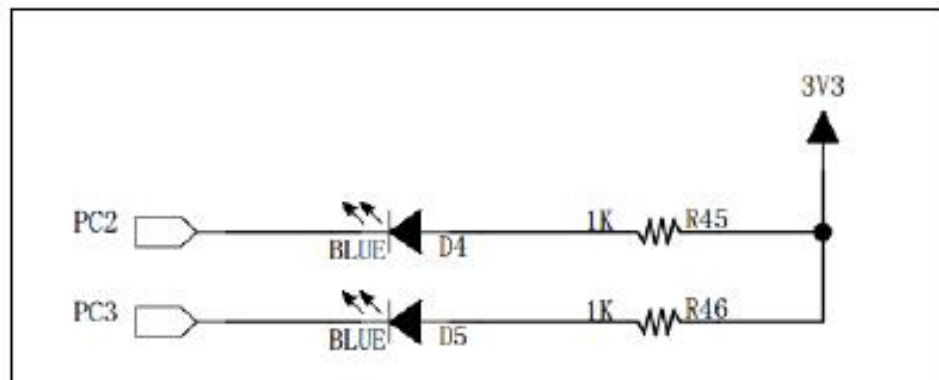
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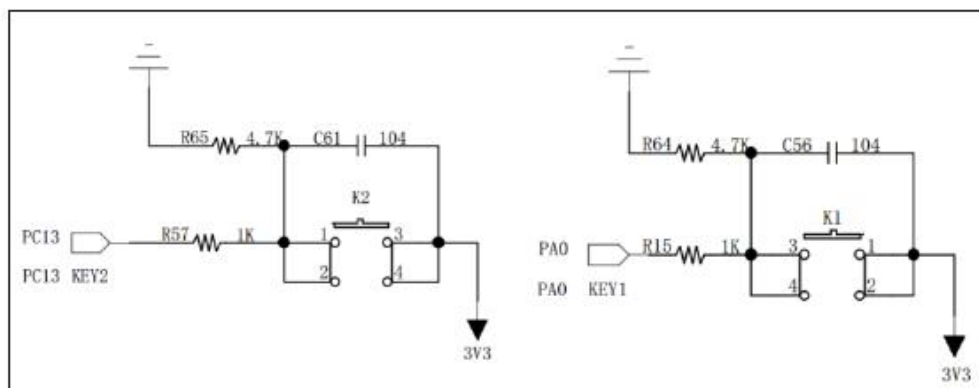
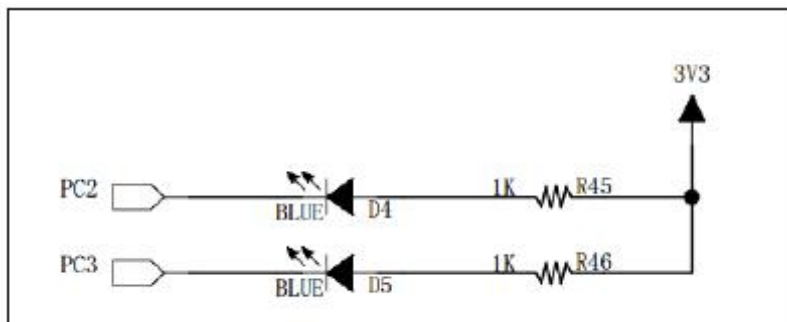
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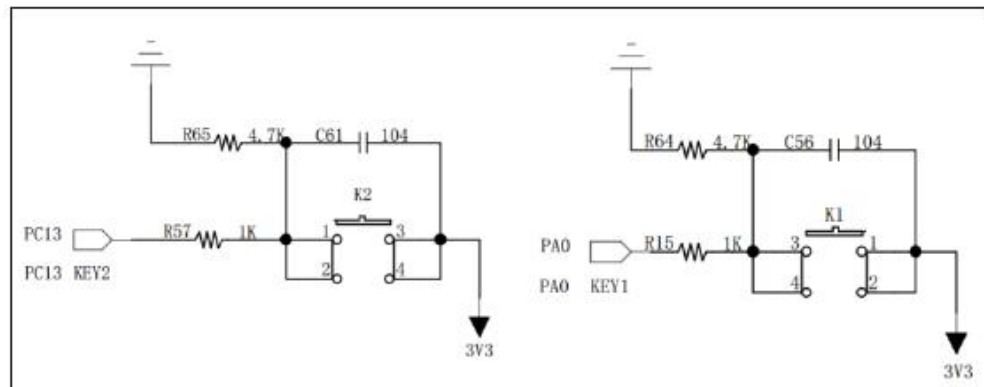
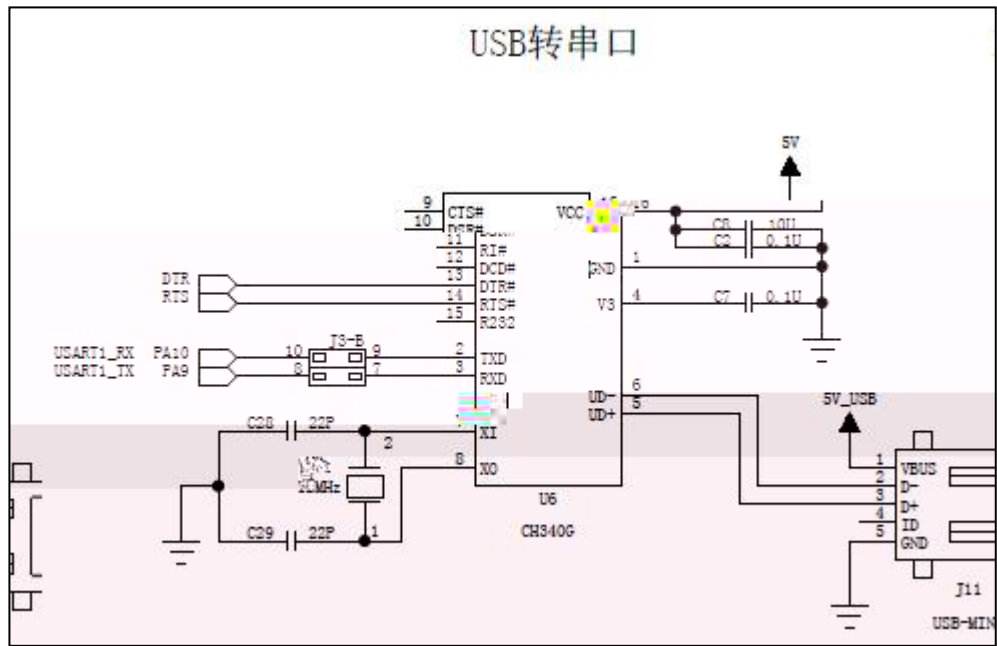


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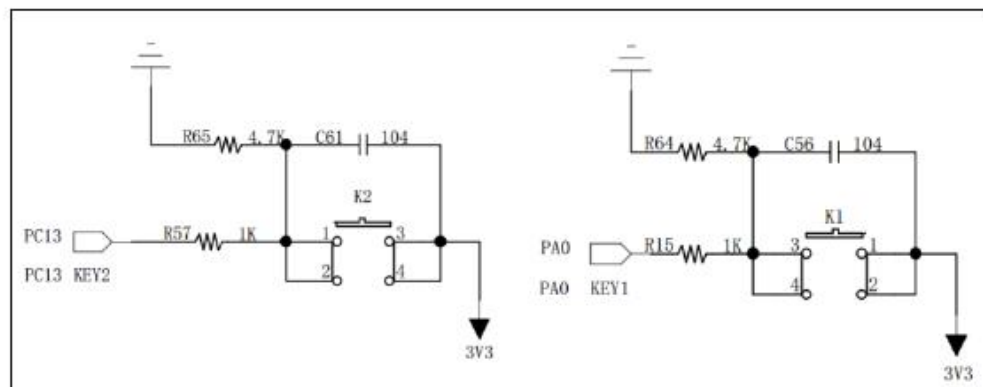
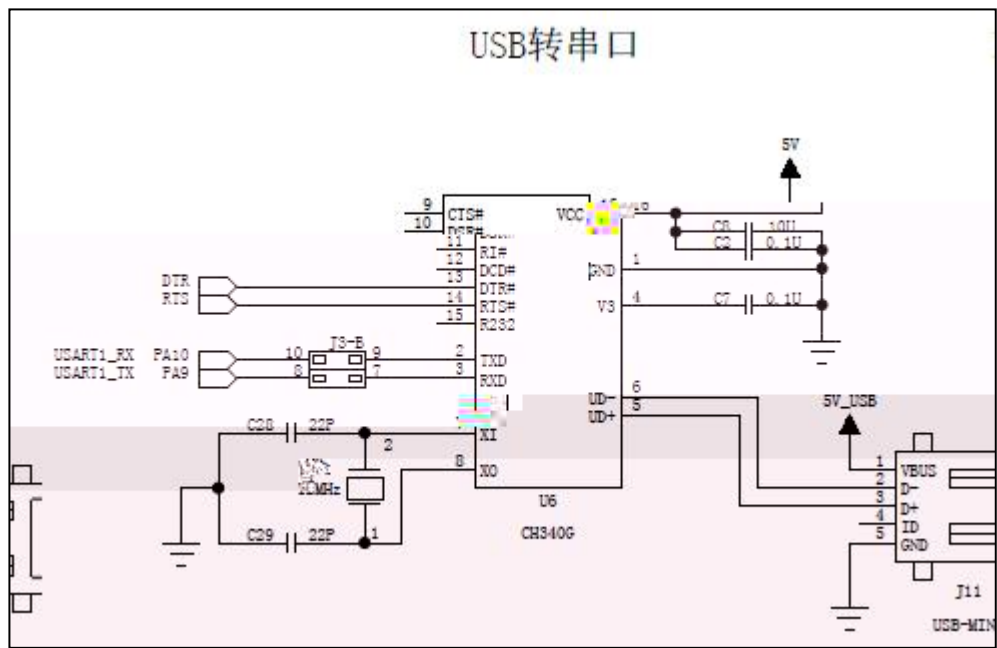


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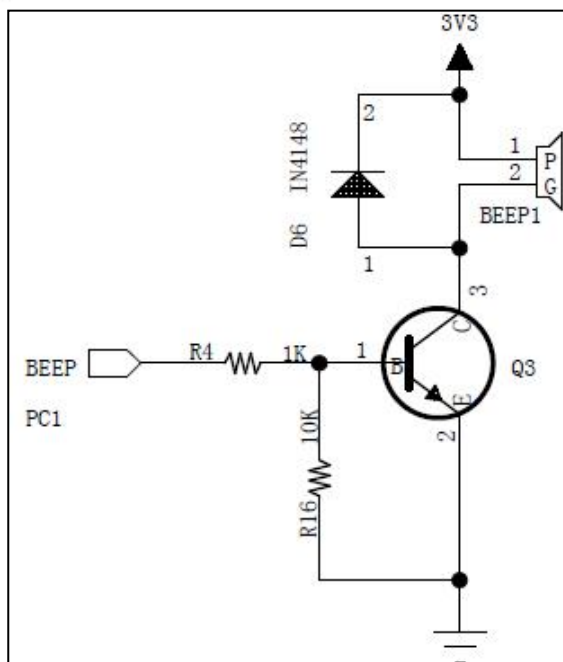


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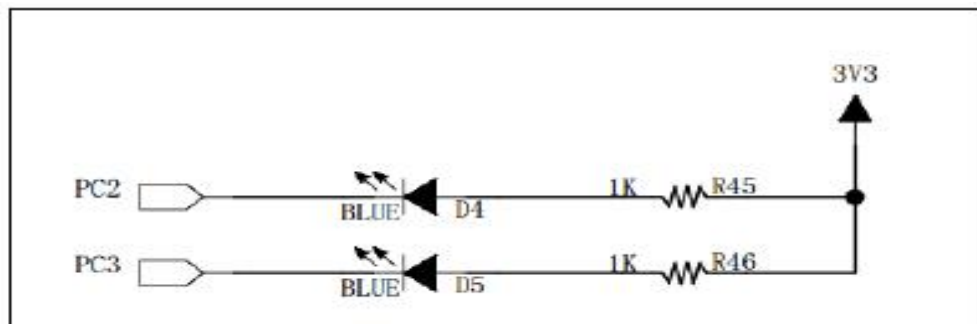


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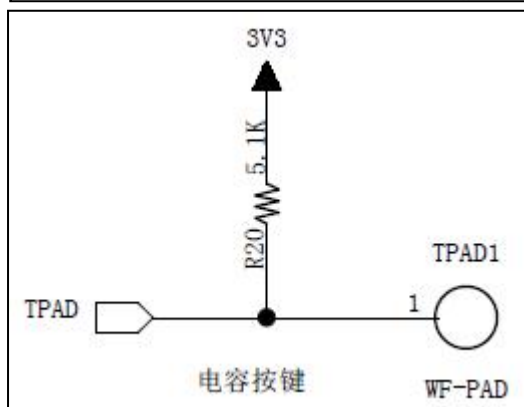
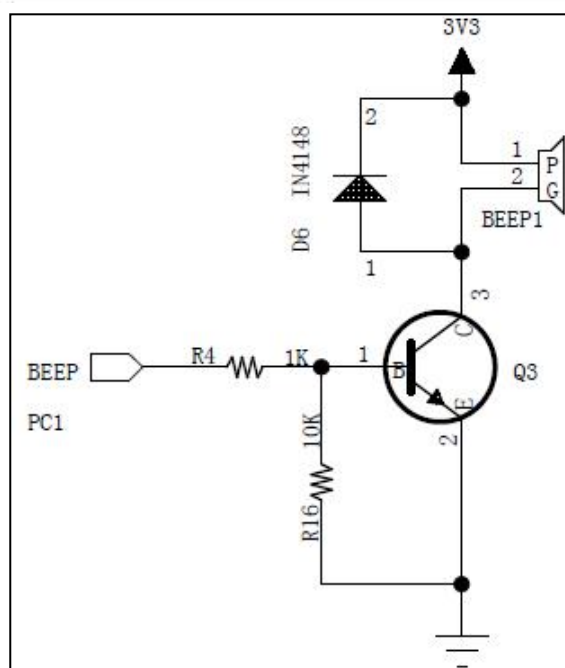
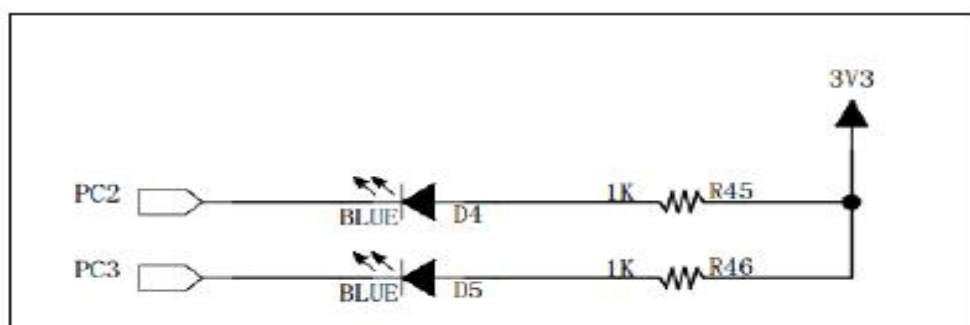
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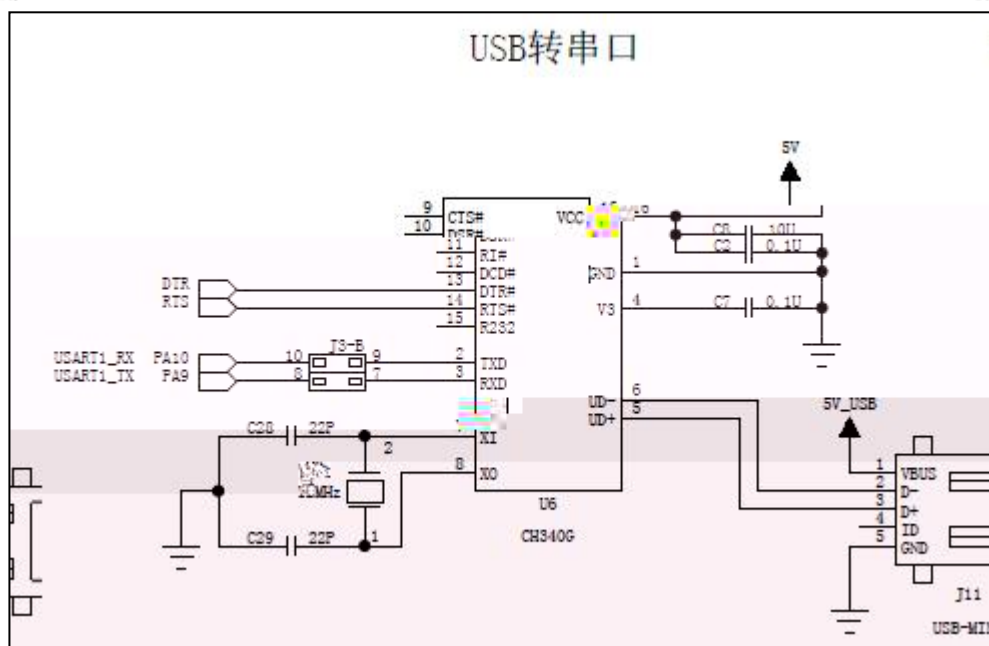
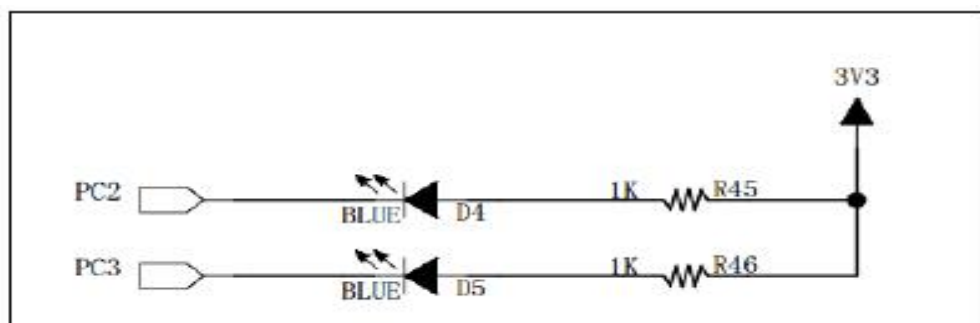
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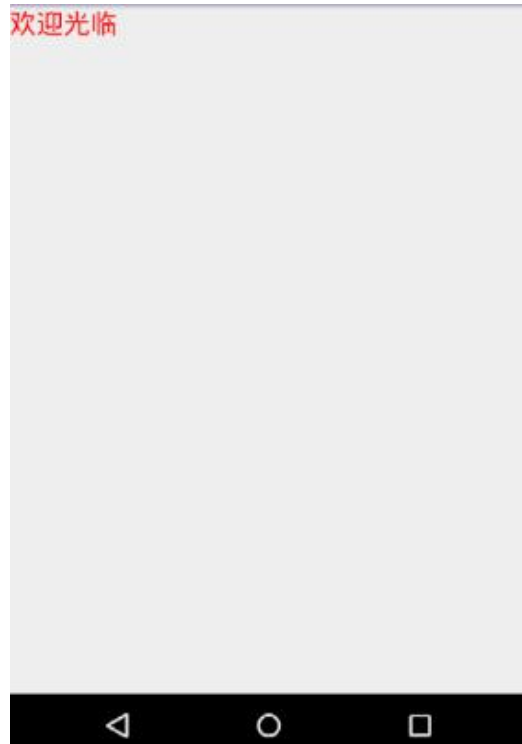
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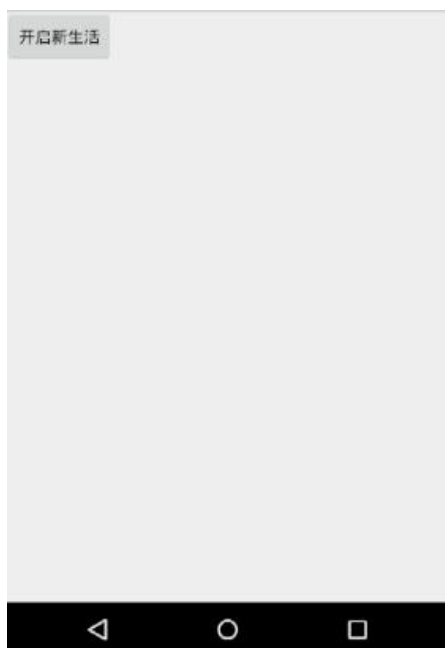
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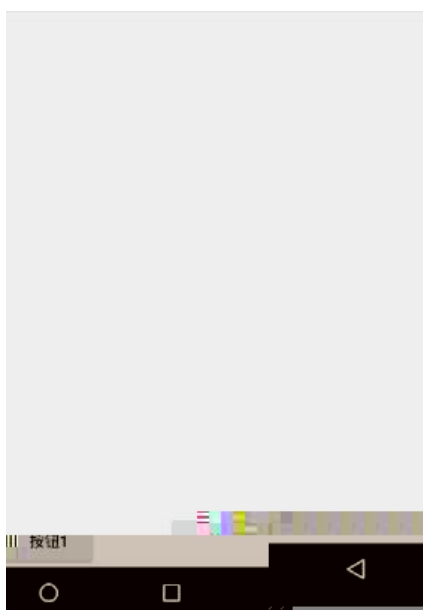
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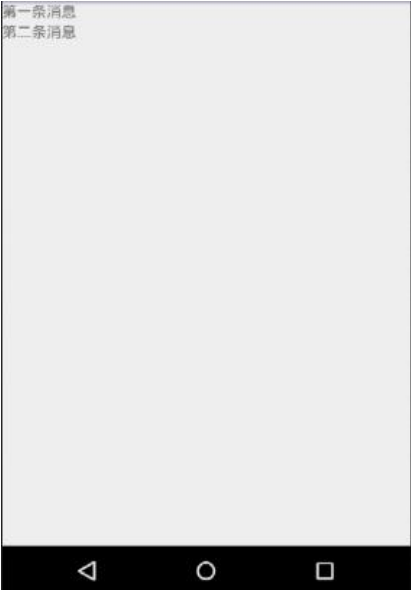
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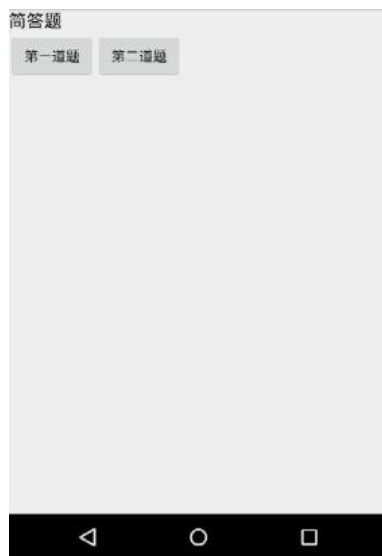


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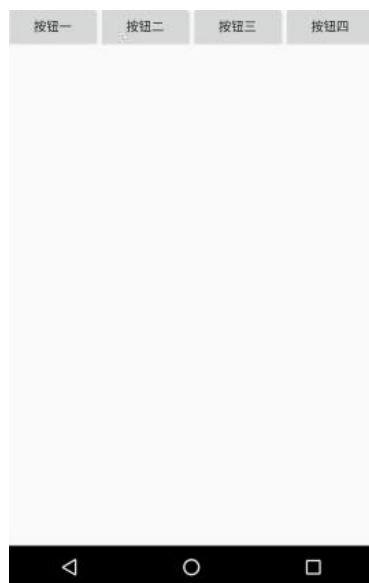
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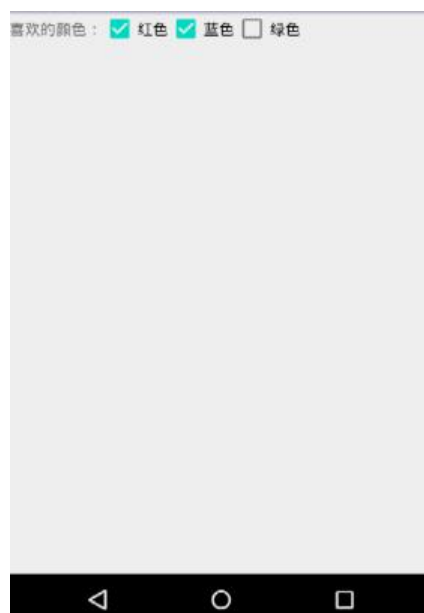
3

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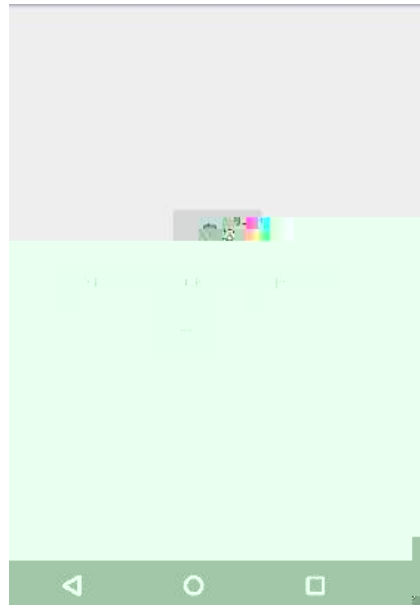


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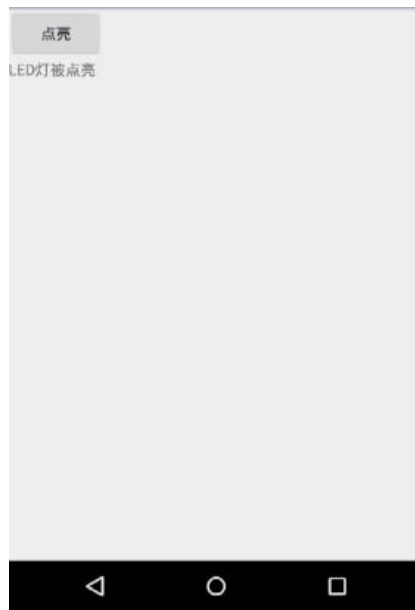
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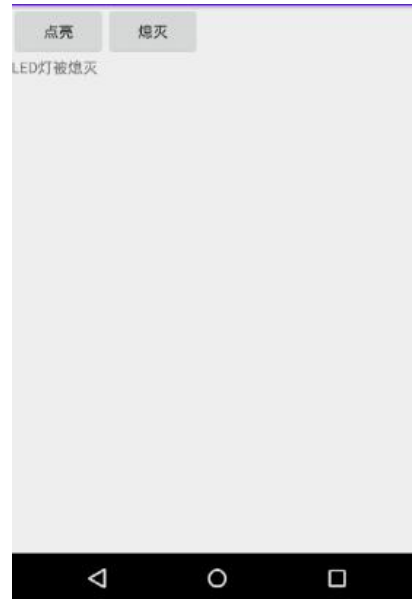
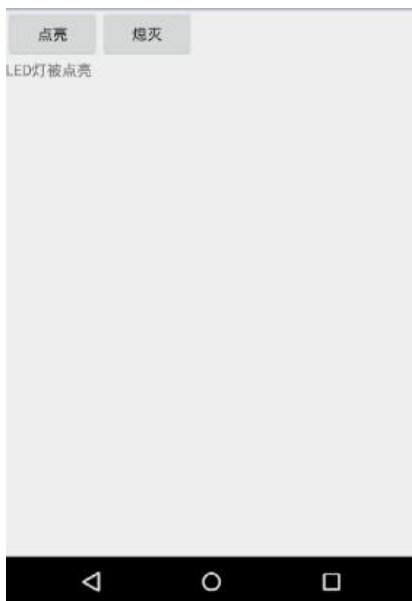
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LED

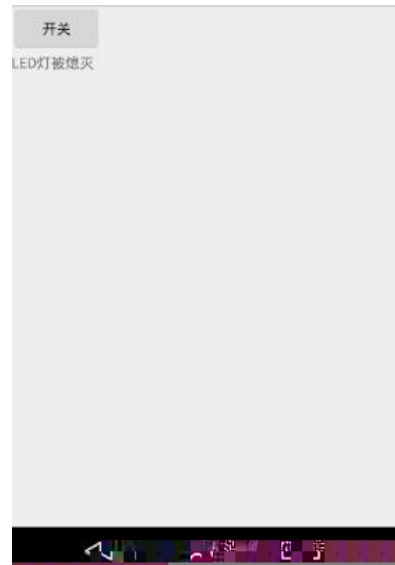
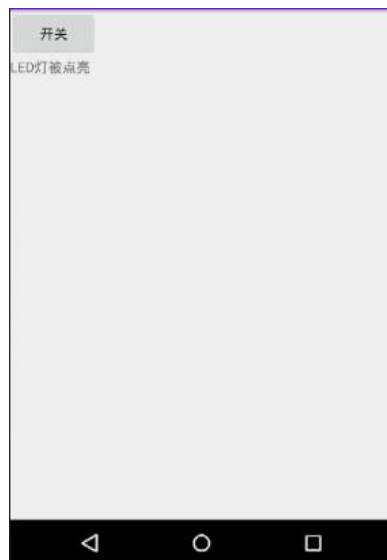
2

1

2

3

TextView LED



3



1

LED

2

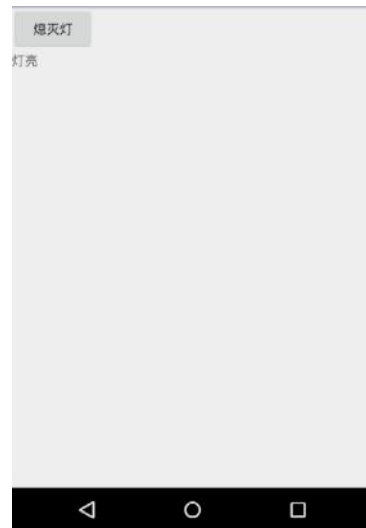
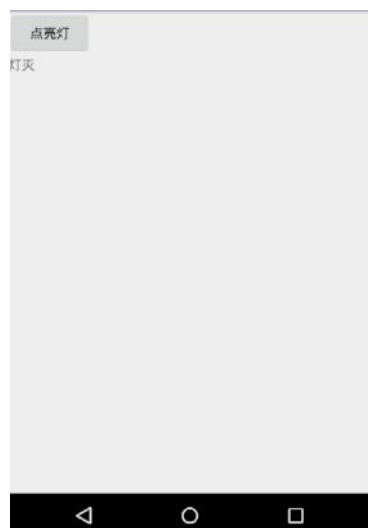
1

2

3

4

TextView



3

1

LED

2

1

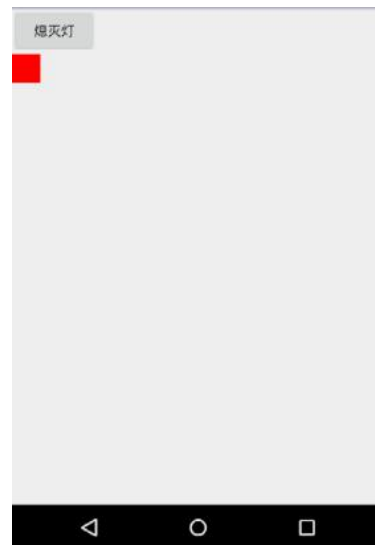
2

3

4

ImageView

30dp\*30dp



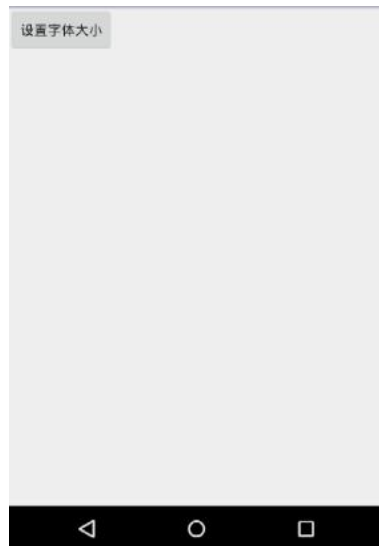
3

1

2

1

2



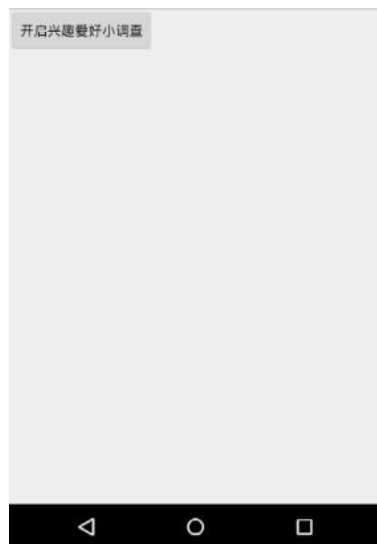
3

1

2

1

2



3